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EXAMINER
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WILLIAMS, HOWARD L

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* FENG CHEN

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Appeal 2007-4279  
Application 10/661,287  
Technology Center 2800

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Decided: May 8, 2008

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Before KENNETH W. HAIRSTON, ROBERT E. NAPPI,  
and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 from the Final Rejection of claims 1-4, 6-12, and 14-17. Claims 5, 13, and 18-20 have been indicated to be allowable by the Examiner (App. Br. 1). We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellant's claimed invention relates to a sigma-delta modulator having a digital feedback signal, and a passive discrete time circuit for 1) receiving the digital feedback signal and an input signal (the input signal comprising information and a pair of analog input currents); 2) converting the digital feedback signal into an analog feedback signal during a first discrete time; and 3) summing the analog feedback signal and a selected one of said pair of analog input currents during a second discrete time to yield a summed signal. The modulator also comprises a passive continuous time circuit having first and second first order filters, and a quantizer. The quantizer is coupled to the continuous time circuit to generate the digital signal, the digital signal comprising the information and determining the selected one of said pair of input signals. (Specification 9:19 to 13:25).

Claim 1 is illustrative of the invention and reads as follows:

1. A sigma-delta modulator, comprising:

a digital feedback signal source for providing a digital feedback signal;

a passive discrete time circuit for receiving the digital feedback signal and an input signal, the input signal comprising information and a pair of analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of said pair of analog input currents during a second discrete time to yield a summed signal;

a passive continuous time circuit comprising a plurality of passive resistive and capacitive elements, the continuous time circuit coupled to the discrete time circuit to filter the summed signal using a first first-order filter

containing resistive and capacitive elements serially connected to a second first order filter containing resistive and capacitive elements to form a second first order filter to generate a filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements, and

a quantizer coupled to the continuous time circuit to generate the digital signal using the filtered signal, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

The Examiner relies on the following prior art references to show unpatentability:

Voorman	US 5,103,228	April 7, 1992
Yamakido	US 5,227,795	July 13, 1993

Philippe Benabes, et al. (“Benabes”), *Passive Sigma-Delta Converters Design*, IEEE Instrumentation and Measurement Technology Conference Record, Anchorage, AK, 469-474, May 21-23, 2002.

Feng Chen, et al. (“Chen”), *A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input*, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, 774-782, June 1997.

Claims 1-4, 6-12, and 14-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Benabes, Chen, and either Voorman or Yamakido.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs and Answer for the respective details.<sup>1</sup> Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived *see* 37 C.F.R. § 41.37 (c) (1) (vii).

## ISSUES

Under 35 U.S.C § 103(a), with respect to appealed claims 1-4, 6-12, and 14-17, would one of ordinary skill in the art at the time of the invention have found it obvious to combine Benabes with Chen and either Yamakido or Voorman to render the claimed invention unpatentable?

## PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). “[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability.” *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore, “there must be some articulated reasoning

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<sup>1</sup> We refer to the Appeal Brief, filed September 7, 2006; Reply Brief, filed May 21, 2007, and Answer, filed April 18, 2007.

with some rational underpinning to support the legal conclusion of obviousness' . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int’l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007)(quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

### 35 U.S.C. § 103(a) REJECTION

We do not sustain the Examiner’s obviousness rejection of claims 1-4, 6-12, and 14-17. The Examiner has not addressed Appellant’s argument that the combination of references does not disclose the claim limitation “said digital signal determining the selected one of said pair of input signals.”<sup>2</sup> (App. Br. 6; *see* Ans. 4-5). That is, Appellant’s state:

All of the rejected independent claims (claims 1, 9 and 17) require a pair of analog input currents with the selection of the one of the pair of input currents being responsive to the digital output of the quantizer. No such feature is taught or suggested by any of the cited references.

(App. Br. 6).

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<sup>2</sup> We determine the “selected one of said pair of input signals” to refer to the “selected one of said pair of analog input currents” in claims 1 and 17, and to the “selected one of the analog input currents” in claim 9.

Appellant repeats the above argument in the Reply Brief, correctly noting, in our view, that the Examiner did not address it. (Reply Br. 1-2). We also do not find the argued limitation addressed in the Examiner's statement of rejection (*see* Ans. 3-4).

On the record before us, the Examiner has not advanced an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" as required by *KSR*, 127 S. Ct. at 1741 (quoting *In re Kahn*, 441 F.3d at 988). This being the case, the Examiner has not established a *prima facie* case of obviousness. Since the resolution of this issue is dispositive of the appeal, we do not address Appellant's further arguments.

Accordingly, we will not sustain the Examiner's rejection of claim 1 on appeal, nor claims 2-8 dependent thereon. Because independent claims 9 and 17 have a similar limitation to the argued limitation in claim 1 discussed *supra* (*see* n. 2), it follows that we also will not sustain the Examiner's rejection of claims 9 and 17, and claims 10-12 and 14-16 dependent from claim 9.

## CONCLUSION

In summary, we do not sustain the Examiner's rejection of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 1-4, 6-12, and 14-17 is reversed.

Appeal 2007-4279  
Application 10/661,287

REVERSED

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